REMARKS

With this current Reply, no claims are either canceled or added. Claims 1-21, 24-26, 28-35, 38-40, and 52-59 therefore continue to be presented for examination.

With respect to claims 1, 11, 19, and 38:

The "Refresh Flags" of Ohsawa are located between the "Decoder" and the "DRAM Cell Array" (Page 84, Figure 5).

Consequently, it is respectfully submitted that no art of record, either alone or in combination, anticipates or renders obvious at least the following elements in conjunction with the other elements of their respective claims:

With respect to claim 1: **A memory controller comprising . . . one or more dynamically changeable use registers corresponding respectively to groups of one or more memory cells of the at least one memory device, wherein the use registers are configurable to indicate whether the corresponding groups of memory cells are in use.**

With respect to claim 11: **a memory controller including one or more dynamically changeable use registers corresponding respectively to groups of one or more memory cells, wherein the use registers are programmable to indicate whether the corresponding groups of memory cells are in use.**

With respect to claim 19: **one or more memory devices having dynamically refreshable memory cells . . . one or more dynamically**

changeable use registers corresponding respectively to groups of one or more memory cells, wherein the use registers are configurable to indicate whether the corresponding groups of memory cells are in use . . . wherein the use registers are not implemented on a same device as the memory cells.

With respect to claim 38: **A memory controller configured to perform actions comprising . . . receiving internal notifications regarding which memory cells are in use based on data stored in a plurality of use registers located on the memory controller.**

With respect to claims 25 and 52:

"Operating system" is only nominally mentioned in Ohsawa (Page 84, Right Column, Item (1)).

Consequently, it is respectfully submitted that no art of record, either alone or in combination, anticipates or renders obvious at least the following elements in conjunction with the other elements of their respective claims:

With respect to claim 25: **a memory controller . . . an operating system configured to dynamically allocate and de-allocate the memory and to identify allocated and de-allocated memory to the memory controller based on whether or not virtual-to-physical memory mapping portions are active . . . wherein the memory controller is responsive to the operating system to operate non-allocated memory at reduced power.**

With respect to claim 52: **receiving memory allocation and de-allocation notifications from an operating system . . . periodically refreshing memory cells that are allocated . . . omitting refreshing of memory cells that are de-allocated . . . wherein the memory allocation and de-allocation notifications are based on virtual memory mapping portions.**

With respect to claim 32:

With respect to "SRA scheme for Cache Memory System", Ohsawa reads, "the system which provides a write-back cache can stop refreshing to a row if all cache lines of the row would became dirty (see Figure 6). This is because each of these cache lines will be written back inevitably." (Page 85, Left Column, Section 3.2).

Consequently, it is respectfully submitted that no art of record, either alone or in combination, anticipates or renders obvious at least the following elements in conjunction with the other elements of their respective claims:

With respect to claim 32: **indicating that memory rows, which have been transferred to a cache, are not in use upon transfer to the cache.**

CONCLUSION

It is respectfully submitted that all of claims 1-21, 24-26, 28-35, 38-40, 52-59 are allowable, and prompt action to that end is hereby requested. Should any matter in this case remain unresolved, the undersigned attorney respectfully requests a telephone conference with the Examiner to resolve any such outstanding matter.

Respectfully Submitted,

Dated: 7/19/2004 By: Keith W. Saunders

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